Features

- Used with the DC003, DC005, and DC006 circuits to implement a program control device interface.
- Used with the DC003, DC005, DC006, and DC010 circuits to implement a direct memory access interface.
- Controls data transfers to and from as many as four 8-byte word registers.
- Provides variable-delay logic for device response to transfer requests.
- Includes Q-bus drivers and receivers.

Description

The DC004 register selector, contained in a 20-pin dual-inline package (DIP), provides the signals to control the transfer of data to and from as many as four word registers (8-bytes). The Q-bus signals directly connect to high-impedance receivers and to high-current drivers on the DC004. A resistor and capacitor circuit (RC) is included to delay the response of the peripheral interface to the data transfers. An external RC network can be added to vary the delay time to conform to the device requirements. Figure 1 is a simplified logic diagram of the DC004 which includes bus latching circuits, enable logic, and a decoder used to select the registers.

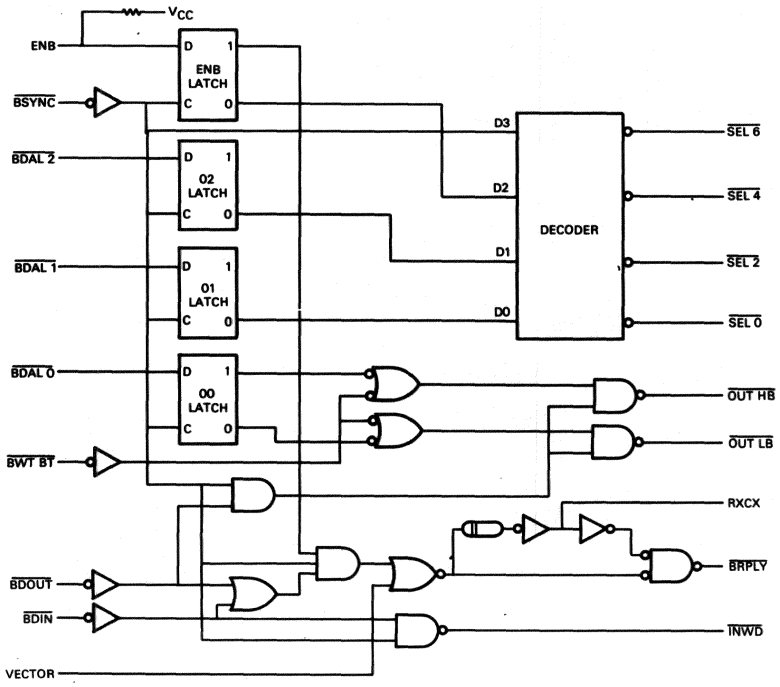


Figure 1 • DC004 Simplified Logic Diagram

• Pin and Signal Descriptions

This section provides a brief description of the input and output signals and power and ground connections of the DC004 20-pin DIP. The pin assignments are identified in Figure 2 and the summarized in Table 1. The signal names shown in the diagram are for the condition where the DC004 is connected to the internal three-state bus of the DC005.

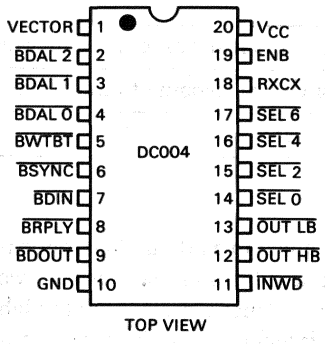


Figure 2 • DC004 Pin Assignments

Table 1 • DC004 Pin and Signal Summary

Pin	Signal	Input/Output	Definition/Function
1	VECTOR	input[1]	Interrupt vector gating—Asserted by the interrupt logic (DC003) to gate the appropriate vector address onto the bus. This signal generates the BRPLY output signal to the bus after a time delay selected by the RC network connected to pin 18 (RXCX).
2-4	BDAL<2:0>	input[2]	Bus data/address lines—The information on these lines is latched by the BSYNC signal from the bus and used to select one or more of the 8-bit registers connected to the SEL 0, SEL 2, SEL 4 and SEL 6 lines.
5	BWTBT	input[2]	Write/Byte—Selects a byte or word operation when the BDOUT signal is asserted: BWTBL asserted = byte, BWTBL negated = word. The latched output of this signal is gated with BDOUT to select a low-byte or high-byte output.
6	BSYNC	input[2]	Bus synchronize—Asserted by the bus master to indicate that an address is on the bus. When unasserted, it disables all the outputs except the vector generated output of BRPLY.
7	BDIN	input[2]	Bus data in—Asserted by the bus master to effect a data input transaction when the BSYNC signal is asserted. It generates the BRPLY output through the delay circuit and the INWD output.
8	BRPLY	output[3]	Bus reply—Asserted by the slave device to indicate that data is available on the BDAL bus or that the device has accepted output data from the bus.
9	BDOUT	input[2]	Bus data out—Asserted by the device to indicate that device data is available on the BDAL lines.
10	GND	input	Ground—Common ground connection
11	INWD	output[1]	In word—Asserted to gate the data from a selected register to the bus.
12 13	OUT LB OUT HB	outputs[1]	Out low-byte, Out high-byte—Used to load the low-byte, high-byte, or both bytes of the write data from the selected register onto the bus.
14 15 16 17	SEL 0 SEL 2 SEL 4 SEL 6	outputs[1]	Select decoder 0, 2, 4, and 6 output lines—Selects a word register for a data transaction.
18	RXCX	output[3]	External RC node—The value of the resistor and capacitor network connected to this pin determines the delay of the BRPLY signal.

Pin	Signal	Input/Output	Definition/Function
19	ENB	input[1,4]	Enable—Asserted to enable the $\overline{SEL\ 0}$, $\overline{SEL\ 2}$, $\overline{SEL\ 4}$, and $\overline{SEL\ 6}$ outputs of the decoder and the address term of $\overline{BRPLY}$.
20	V_{CC}	input	Voltage—Power supply dc voltage

[1]TTL level
[2]high-impedence
[3]open-collector
[4]connected to V_{CC} through an 850Ω resistor

• Application Information

Refer to the *Chipkit Users Manual LSI-11 Bus Interface Chips* (document no. EJ-01387-92) for general application information. The Q-bus is an LSI-11 bus.

• Specifications

The mechanical, electrical, and environmental characteristics and specifications for the DC003 are described in the following paragraphs. The test conditions for the electrical values are as follows unless specified otherwise.

- Operating temperature (T_A): 0°C to 70°C
- Supply voltage (V_{CC}): 5.0 V ±5%

Mechanical Configuration

The physical dimensions of the DC004 20-pin DIP are contained in Appendix E. The materials and construction of the molded DIP are defined in Digital Specification A-PS-2100002-GS.

Absolute Maximum Ratings

Stresses greater than the absolute maximum ratings may cause permanent damage to the device. Exposure to the absolute maximum ratings for extended periods may adversely affect the reliability of the device.

- Supply voltage (V_{CC}): 7.0 V
- Input voltage (V_I): 5.5 V
- Operating temperature (T_A): 0°C to 70°C
- Storage temperature (T_S): –65°C to 150°C

Recommended Operating Conditions

- Supply voltage (V_{CC}): 4.75 V (minimum), 5.0 V (normal), 5.25 V (maximum)
- Supply current (I_{CC}): 120 mA (maximum)
- Free-air temperature: 0°C to 70°C
- Relative humidity: 10% to 95% (noncondensing)

dc Electrical Characteristics

The dc electrical characteristics of the DC004 for the operating voltage and temperature ranges specified are listed in Tables 2 through 4. Table 2 lists the dc specifications for the TTL input and outputs that do not connect to the Q-bus bus. Table 3 lists the dc specifications for the high-impedance receiver inputs from the Q-bus bus. Table 4 lists the dc specifications for the open-collector driver outputs that connect to the Q-bus. Refer to Appendix C for test circuit configurations listed in the tables.

- Note: Pin 18 (RXCX) of the DC004 must be connected to V_{CC} through a 1-kΩ ±5% resistor for performing all the dc tests shown in the test circuit diagrams in Appendix C.

Table 2 • DC004 TTL Input and Output Parameters

Parameter	Symbol	Test Condition	Requirements Min	Requirements Max	Units	Test Circuit
High-level input voltage	V_{IH}		2.0	—	V	C1,C2
Low-level input voltage	V_{IL}		—	0.8	V	C1,C2
Input clamp voltage	V_I	V_{CC}=4.75 V I_I=−18 mA	—	−1.2	V	C3
High-level output voltage	V_{OH}	V_{CC}=4.75 I_O=−1.0 mA	2.7	—	V	C1
Low-level output voltage	V_{OL}	V_{CC}=4.75 V I_O=20 mA	—	0.5	V	C2
Input current at maximum input voltage	I_I	V_{CC}=5.25 V V_I=5.5 V[1]	—	1.0	mA	C4
High-level input current	I_{IH}	V_{CC}=5.25 V V_I=2.7 V[1]	—	50	μA	C4

Parameter	Symbol	Test Condition	Requirements Min	Requirements Max	Units	Test Circuit
Low-level input current	I_{IL}	$V_{CC}=5.25$ V $V_I=0.5$ V	—	-0.70	mA	C5
Short-circuit output current	I_{OS}	$V_{CC}=5.25$ V[2]	-40	-100	mA	C6
Supply current	I_{CC}	$V_{CC}=5.25$ V	—	120	mA	C7

[1]Limits for pin 19 are: $I_I=1.4$ mA, $I_H=-2.25$ mA (minimum) and -3.85 mA (maximum), $I_{IL}=-4.5$ mA (minimum) and -8.0 mA (maximum).
[2]Not more than one output shall be shorted at a time and the duration of the short shall not exceed 1 second.

Table 3 • DC004 High-impedance Bus Receiver Parameters

Parameter	Symbol	Test Condition	Requirements Min	Requirements Max	Units	Test Circuit
High-level input voltage	V_{IH}	$V_{CC}=4.75$ V $V_{CC}=5.25$ V	1.53 1.70	— —	V V	C1,C2
Low-level input voltage	V_{IL}	$V_{CC}=4.75$ V $V_{CC}=5.25$ V	— —	1.30 1.47	V V	C1,C2
Input clamp voltage	V_I	$V_{CC}=4.75$ V $I_I=-18$ mA	—	-1.2	V	C3
High-level input current	I_{IH}	$V_I=3.8$ V $V_{CC}=0$ V $V_{CC}=5.25$ V	— —	40 40	µA µA	C4
Low-level input current	I_{IL}	$V_I=0$ V $V_{CC}=0$ V $V_{CC}=5.25$ V	— —	-10 -10	µA µA	C5 C5

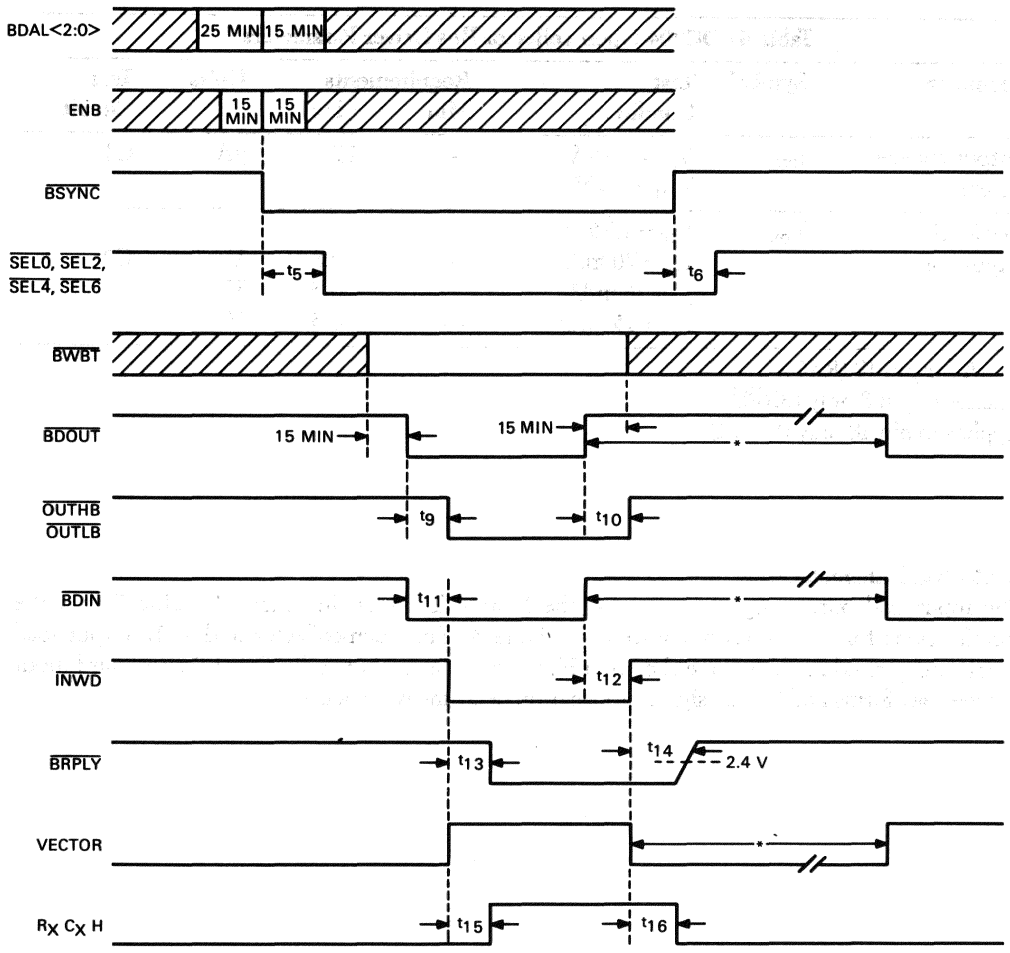
Table 4 • DC004 Open-collector Bus Driver Parameters

Parameter	Symbol	Test Condition	Requirements Min	Requirements Max	Units	Test Circuit
Output reverse current	I_{OH}	V_{CC} = 4.75 V V_{OH} = 3.5 V	—	25[1]	μA	C1
Low-level output voltage	V_{OL}	V_{CC} = 4.75 V I_{sink} = 70 mA[2] $_{sink}$ = 16 mA[3] I_{sink} = 15 mA3	— — —	0.8 0.5 0.5	V V V	C2

[1]65 μA for pin 18 (RXCX).
[2]Applies to pin 8 only ($\overline{\text{BRPLY}}$).
[3]Applies to pin 18 only (RXCX).

ac Electrical Characteristics

The input and output signal timing for the DC004 is shown in Figure 3. Table 5 lists the specifications for the values referenced on Figure 3. The open-collector and TTL output load circuits referenced in Table 5 are shown in Figure 4. Refer to Appendix D for the standard input voltage waveforms and for the signal propagation delay measurements.



*TIME REQUIRED TO DISCHARGE R_X C_X FROM ANY CONDITION ASSERTED = 150 ns.

NOTE
TIMES ARE IN NANOSECONDS.

Figure 3 ▪ DC004 Signal Timing Sequence

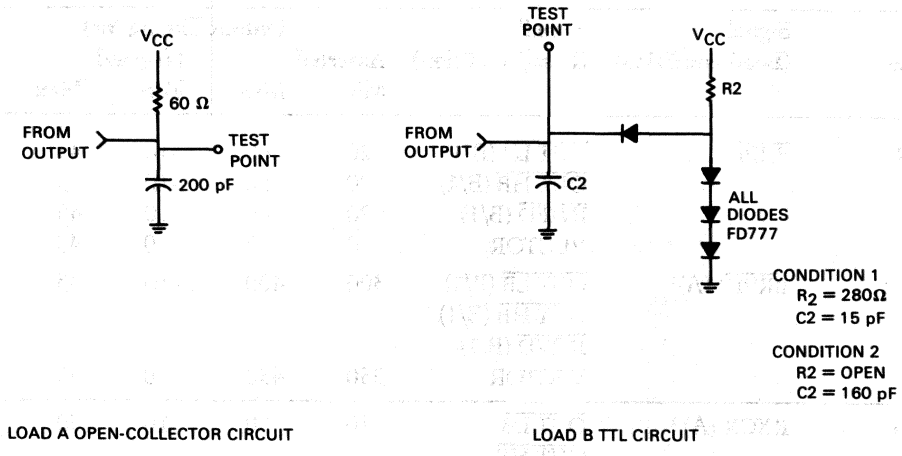


Figure 4 • DC004 Output Load Circuits

Table 5 • DC004 Signal Timing Specifications

Timing Reference	Signal[1] (Load/condition)	Signal[1] (Load/condition)	Output Timing (ns) Asserted Min	Asserted Max	Negated Min	Negated Max
T5,T6	$\overline{\text{SEL 0}}$ (B/2)	$\overline{\text{BSYNC}}$	15	40	5	30
	$\overline{\text{SEL 2}}$ (B/2)		15	40	5	30
	$\overline{\text{SEL 4}}$ (B/2)		15	40	5	30
	$\overline{\text{SEL 6}}$ (B/2)		15	40	5	30
T9, T10	$\overline{\text{OUT LB}}$ (B/2)	$\overline{\text{BDOUT}}$	5	30	5	30
	$\overline{\text{OUT HB}}$ (B/2)		5	30	5	30
T11, T12	$\overline{\text{INWD}}$ (B/2)	$\overline{\text{BDIN}}$	5	30	5	30

Timing Reference	Signal[1] (Load/condition)	Signal[1] (Load/condition)	Output Timing (ns) Asserted Min	Asserted Max	Negated Min	Negated Max
T13, T14	$\overline{\text{BRPLY}}$ (A)[2]	$\overline{\text{OUT LB}}$ (B/1)	20	60	-10	45
		$\overline{\text{OUT HB}}$ (B/1)	20	60	-10	45
		$\overline{\text{INWD}}$ (B/1)	20	60	-10	45
		VECTOR	30	70	0	45
	$\overline{\text{BRPLY}}$ (A)[3]	$\overline{\text{OUT LB}}$ (B/1)	300	400	-10	45
		$\overline{\text{OUT HB}}$ (B/1)				
		$\overline{\text{INWD}}$ (B/1)				
		VECTOR	330	430	0	45
T15, T16	RXCX (A) [2]	$\overline{\text{OUT LB}}$	10	50	10	50
		$\overline{\text{OUT HB}}$				
		$\overline{\text{INWD}}$				
		VECTOR				

[1]Refer to Figure 4 for load circuit configurations.
[2]Pin 18 connections: Rx = 330Ω 5%, Cx = 15 pF 5%.
[3]Pin 18 connections: Rx = 4.64 kΩ 5%, Cx = 220 pF 5%.